Claims

What is claimed is:

1. A processor comprising:

scheduling circuitry for scheduling data blocks for transmission from a plurality of transmission elements, the scheduling circuitry being configurable for utilization of at least one time slot table in scheduling the data blocks for transmission; and

an interval computation element associated with the scheduling circuitry and operative to determine an interval for transmission of one or more data blocks associated with corresponding locations in the time slot table, the transmission interval being adjustable under control of the interval computation element so as to facilitate the maintenance of a desired service level for one or more of the transmission elements.

2. The processor of claim 1 wherein the interval computation element operates under software control in at least one of determining and adjusting the transmission interval.

3. The processor of claim 1 wherein the interval computation element comprises a script processor.

4. The processor of claim 1 wherein the interval computation element is operative to determine periodically if the transmission interval requires adjustment in order to maintain the desired service level for one or more of the transmission elements.

5. The processor of claim 4 wherein the interval computation element makes a determination as to whether the transmission interval requires adjustment, after transmission of a specified number of the data blocks.

6. The processor of claim 5 wherein the interval computation element makes the determination as to whether the transmission interval requires adjustment after transmission of each of the data blocks.

7. The processor of claim 1 wherein the transmission interval specifies a rate at which data blocks associated with corresponding locations in the time slot table are transmitted.

8. The processor of claim 1 wherein the interval computation element is operative to select the transmission interval from at least a first transmission interval associated with a first scheduling algorithm and a second transmission interval associated with a second scheduling algorithm.

9. The processor of claim 1 wherein a given requesting transmission element is assigned to a location in the time slot table in accordance with the following equation:

$$\text{Assigned Time Slot} = \text{Current Time} + \text{Interval},$$

where Current Time denotes a time corresponding to a current transmission time slot and Interval denotes the transmission interval.

10. The processor of claim 1 wherein the scheduling circuitry comprises the time slot table.

11. The processor of claim 1 further comprising traffic shaping circuitry coupled to the scheduling circuitry, the traffic shaping circuitry comprising the interval computation element.

12. The processor of claim 11 further comprising transmit queue circuitry coupled to the scheduling circuitry, wherein the transmission elements comprise one or more queues associated with the transmit queue circuitry, the transmit queue circuitry supplying time slot requests from the transmission elements to the scheduling circuitry in accordance with a traffic shaping requirement established by the traffic shaping circuitry.

13. The processor of claim 1 wherein the time slot table is stored at least in part in an internal memory of the processor.

14. The processor of claim 1 wherein the time slot table is stored at least in part in an external memory coupled to the processor.

15. The processor of claim 1 wherein one or more of the data blocks comprise data packets.

16. The processor of claim 1 wherein the scheduling circuitry provides dynamic maintenance of the time slot table such that identifiers of requesting transmission elements are entered into the table locations on a demand basis.

17. The processor of claim 16 wherein the identifiers of the transmission elements comprise a structure having one or more bits for allowing a given one of the transmission element identifiers to be linked to another of the transmission element identifiers.

18. The processor of claim 1 wherein the processor comprises a network processor configured to provide an interface for data block transfer between a network and a switch fabric.

19. The processor of claim 1 wherein the processor is configured as an integrated circuit.

20. A method for use in a processor, the method comprising:

scheduling data blocks for transmission from a plurality of transmission elements;

wherein the scheduling step utilizes at least one time slot table to schedule the data blocks for transmission in accordance with a determined interval for transmission of one or more data blocks associated with corresponding locations in the time slot table, the transmission interval being adjustable so as to facilitate the maintenance of a desired service level for one or more of the transmission elements.

21. An article of manufacture comprising a machine-readable storage medium for use in conjunction with a processor, the medium storing one or more software programs for use in scheduling data blocks for transmission from a plurality of transmission elements utilizing at least

one time slot table, the one or more programs when executed providing at least one of determination of an interval for transmission of one or more data blocks associated with corresponding locations in the time slot table and adjustment of the interval so as to facilitate the maintenance of a desired service level for one or more of the transmission elements.